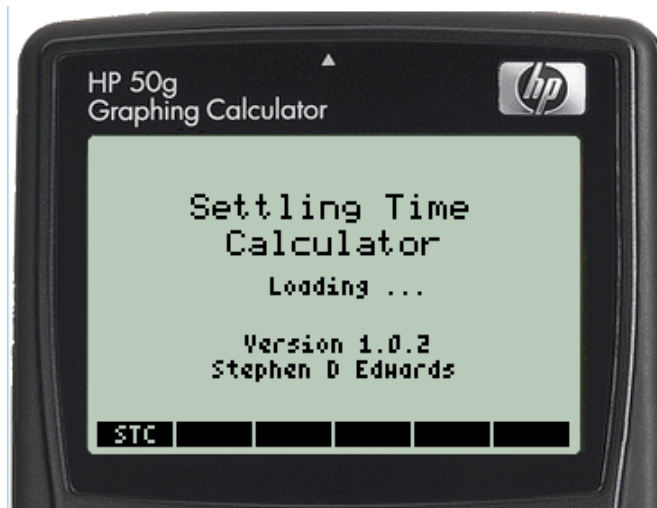


SETTLING TIME CALCULATOR USER'S GUIDE



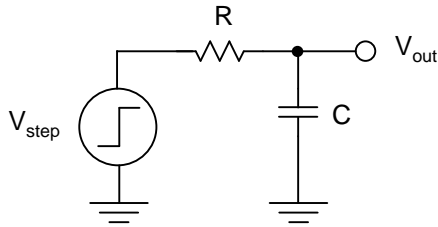
Stephen D. Edwards
Maxim Integrated

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SECTION 1 - INTRODUCTION

Settling Time Calculator (STC) is a program written for the HP50g calculator that aids in the analysis and design of the step response of a single pole RC filter. STC finds the time it takes (**ts**) for the output voltage to respond to a step input voltage (**Vstep**) and settle to within a specified fraction (**Accu**) of the final value.



Each parameter can be entered or found. STC can also be run on a PC using the free program HPUseEdit 5.4, found at www.hpcalc.org, or the calculator page at www.maximintegrated.com.

Ten parameters can be entered or found,

- Resistance, **R**, in $k\Omega$
- Capacitance, **C**, in nF
- Settling Time, **ts**, in μs
- Accuracy, **Accu**, in τ
- Accuracy, **Accu**, in PPM
- Accuracy, **Accu**, in %
- Accuracy, **Accu**, in μV
- Accuracy, **Accu**, in LSB
- Voltage Step Size, **Vstep**, in V
- Resolution, **Res**, in bits

STC can find any of these parameters as a function of the others, making it useful for both design and analysis.

Three additional circuit parameters are found,

- Time Constant, **τ** , in μs
- Cutoff Frequency, **Fc**, in kHz
- Rise Time, **tr**, in μs

These parameters appear in STC as shown below:

```
R = 1.0000 kΩ
C = 1.0000 nF
ts = 11.5129 μs
Accu = 11.5129 τ
Accu = 10.0000 PPM
Accu = 100.0000 μV
Vstep = 10.0000 V
τ = 1.0000 μs
NAME STO RCL PLOT FIND EXIT
```

with alternative
parameters,

```
R = 1.0000 kΩ
C = 1.0000 nF
ts = 11.5129 μs
Accu = 11.5129 τ
Accu = 0.0010 %
Accu = 0.0102 LSB
Res = 10.0000 bit
Fc = 1591.5494 kHz
NAME STO RCL PLOT FIND EXIT
```

Refer to Section 7 for an explanation of the parameters and how they are calculated.

SECTION 2 - INSTALLATION

STC can be installed on the HP50g calculator or a Windows PC.

Installing STC on the HP50g Calculator

STC may be installed in any one of three ways:

A. Best when installing one calculator:

Copy the executable file STC.hp to the home directory or subdirectory of the HP50g calculator. Launch STC.hp.

B. Best when installing two to six calculators:

Copy the executable file STC.hp to the root directory of an SD card, and the much smaller file STC to the home directory or subdirectory of the HP50g calculator. Launch STC.

C. Best when installing six or more calculators:

Install STC using the Calculator Launcher (CALC) utility found at www.maximintegrated.com/design/tools/calculators/hp50g/. Refer to the CALC User's Guide for an explanation of this utility

Refer to the HP50g Graphing Calculator User's Guide for instructions on how to copy files to the calculator.

Installing STC on a Windows PC


STC can be run on a Windows PC using the free program HPUserEdit 5.4. HPUserEdit is an IDE for the HP50g and contains a suitable emulator.

To install HPUserEdit:



Download and install HPUserEdit 5.4, found at www.hpcalc.org. Search for "HPUserEdit5". The default language is Spanish. However, other languages can be selected as follows,

1. Select 'Opciones' (Options)
2. Select 'Idiomas' (Language)
3. Select the preferred language (English is assumed in this document)

To run STC:

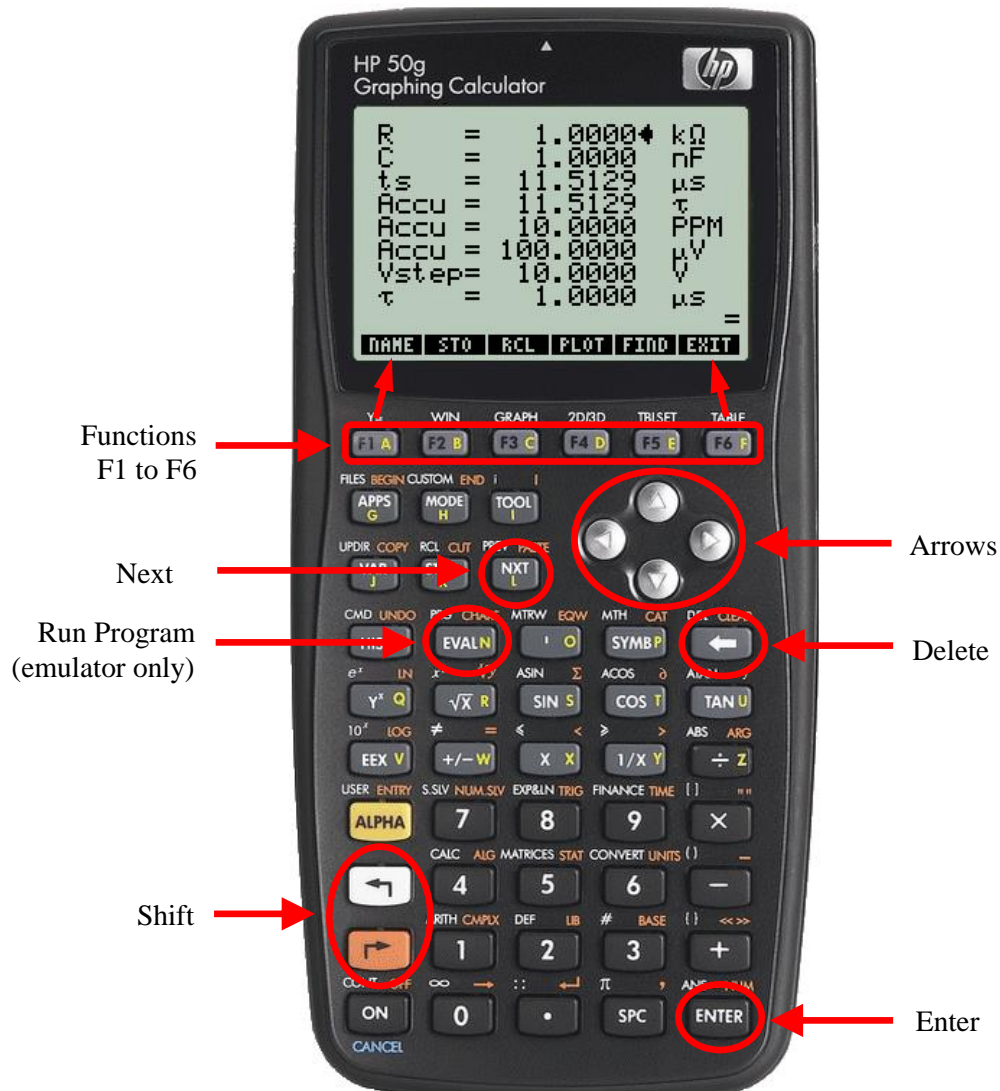
1. Launch HPUserEdit
2. Launch the HP50g emulator by selecting Emulator/Run_the_Emulator from the menu bar. A virtual HP50g appears.
3. Drag and drop STC.hp from an *unzipped* folder to the calculator screen and click the  key.

The splash screen shown on page 1 of this guide is displayed when the calculator is loading. It appears momentarily, and may not be visible when run on a PC.

STC creates a file named 'CalcDB' in the calculator's home directory the first time it is run. 'CalcDB' holds the parameter values used by STC when launched, and is used by the  and  commands to store and recall the parameters.

SECTION 3 - KEYBOARD

The following diagram shows the location of all keys used by STC:



When using the emulator, the calculator keys map to the PC keyboard as follows:

Calculator Keys	↔	PC Keyboard
Numbers	↔	Numbers
Enter and Delete	↔	Enter and Delete
Yellow Letters	↔	Letters
Arrows	↔	Arrows
Left Shift	↔	Shift
Right Shift	↔	Control

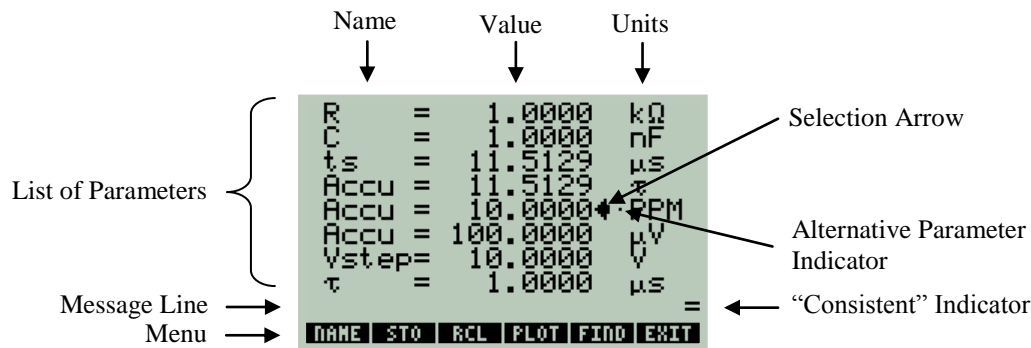
SECTION 4 - COMMANDS

STC has four sets of commands:

- Main Menu Commands
- Extended Menu Commands
- Help Commands
- Plot Commands

Main Menu Commands

After launching STC for the first time, the following screen appears, listing eight parameters.



Use the and keys to select a parameter.

Use the key to display an alternative parameter where a “.” appears right of the selection arrow.

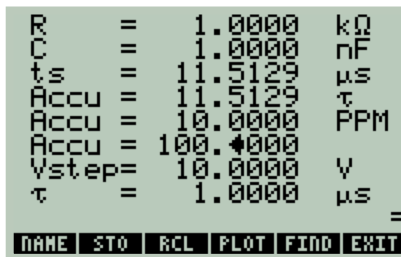
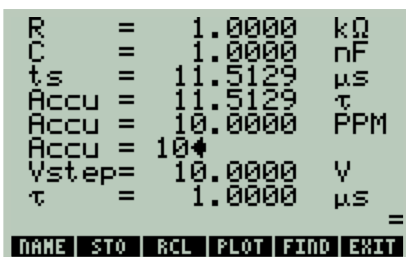
Use the (insert) or (delete) key to enter or edit a parameter. Press when finished.

- () Display the name of the selected parameter in the message line
- () Display the full precision of the selected parameter in the message line
- () Store all parameters
- () Recall all stored parameters
- () Plot the step response
- () Find the selected parameter
- () Exit the program
- (Cancel) Exit the program
- () Launch previous run calculator (for physical calculators only - requires CALC)
- () Turn off the calculator


Enter or edit a parameter value by using one of the following keys:

the delete key (),



and the left arrow (insert) key ()

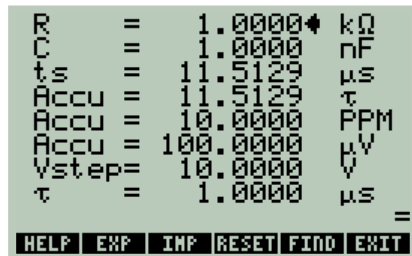






Press when finished.

The equal sign (=), in the lower right hand corner of the display, indicates that all the parameters are consistent with each other. That is, an RC filter with component values **R** kilohms and **C** nanofarads will settle to an accuracy of **Accu** (in PPM, %, uV, LSB, or τ) in **ts** microseconds, and have a time constant of τ microseconds, a cutoff frequency of **Fc** kilohertz, and a rise time of **tr** microseconds. The parameters are always consistent immediately following a **F5** () command, and the “=” will appear. Any entry of a parameter value will show the “≠” sign, indicating that the parameters may no longer be consistent.

Extended Menu Commands





Press the **NXT** () key to display the Extended Menu showing four additional commands. Press **NXT** () again to return to the Main Menu.

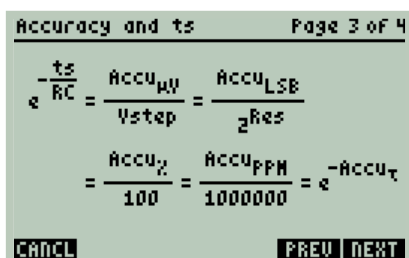
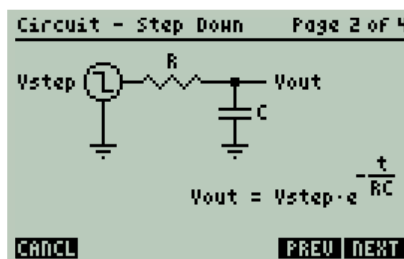
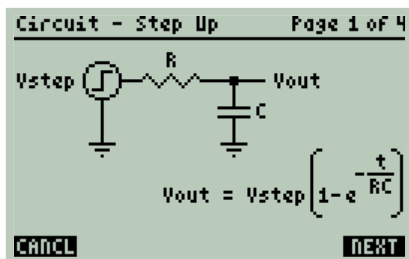


- F1** () Display the settling time equations used by STC
- F2** () Export the selected parameter to the stack upon exiting
- F3** () Import the number present in level 1 of the stack when STC was launched to the selected parameter
- F4** () Enter all default parameter values

The Main Menu reappears after executing an extended menu command.

Help Command

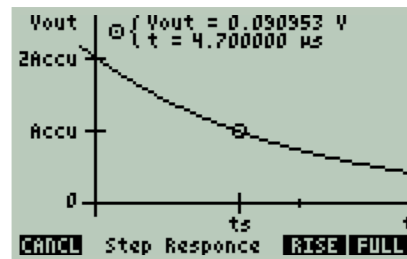
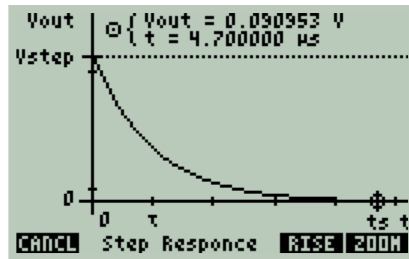
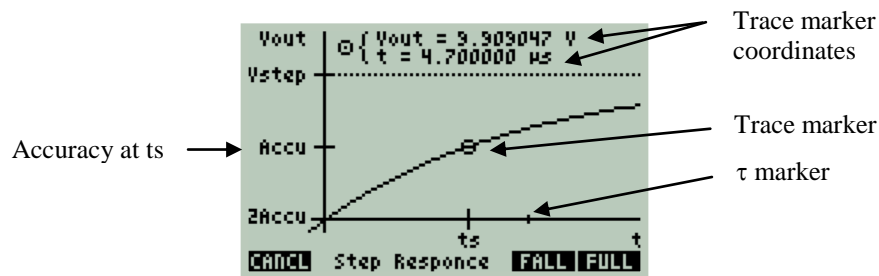
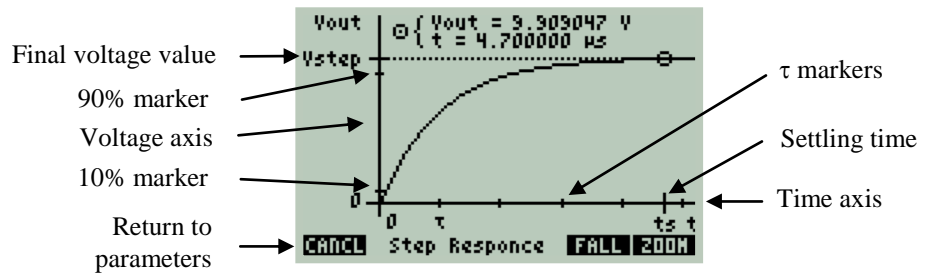
Press **F1** () to display the help screen, and **F5** () and **F6** () to view pages 1 through 4 shown below. Press **F1** () to return to the parameter display.








Plot Commands











 (F4 in the Main Menu) plots the step response of an RC filter.

The key elements of the plot display are show below:



The following keys are active when a plot is displayed:

- (F1)  Return to the parameter display
- (F5)  Display a falling step
- (F5)  Display a rising step
- (F6)  Plot the full settling time (0 to ts)
- (F6)  Plot the time range between $\frac{1}{2} \cdot \text{Accu}$ and $2 \cdot \text{Accu}$


-   Move trace marker left by 1 pixel
-  Move trace marker left by 10 pixel
-   Move trace marker left to the closest marker
-   Move trace marker right by 1 pixel
-  Move trace marker right by 10 pixel
-   Move trace marker right to the closest marker

SECTION 5 - MESSAGES

STC displays five types of messages on the message line:

1. Name Messages

```
R      = 1.0000 kΩ
C      = 1.0000 nF
ts     = 11.5129 μs
Accu   = 11.5129 τ
Accu   = 10.0000 PPM
Accu   = 100.0000 μV
Vstep  = 10.0000 V
τ      = 1.0000 μs
Voltage Step Size =
NAME STO RCL PLOT FIND EXIT
```

Name messages describe the selected parameter when  is active.

2. Busy Messages

```
R      = 1.0000 kΩ
C      = 1.0000 nF
ts     = 11.5129 μs
Accu   = 11.5129 τ
Accu   = 10.0000 PPM
Accu   = 100.0000 μV
Vstep  = 10.0000 V
τ      = 1.0000 μs
Finding ... =
NAME STO RCL PLOT FIND EXIT
```

Busy messages explain what the program its doing.



3. Error Messages

```
R      = 1.0000 kΩ
C      = 1.0000 nF
ts     = 11.5129 μs
Accu   = 11.5129 τ
Accu   = 10.0000 PPM
Accu   = 100.0000 μV
Vstep  = 10.0000 V
τ      = 1.0000 μs
Zero or Negative Not Allowed! =
NAME STO RCL PLOT FIND EXIT
```

Error messages warn of an illegal entry, command, or result.

4. Full Precision Messages

```
R      = 1.0000 kΩ
C      = 1.0000 nF
ts     = 11.5129 μs
Accu   = 11.5129 τ
Accu   = 10.0000 PPM
Accu   = 100.0000 μV
Vstep  = 10.0000 V
τ      = 1.0000 μs
Precisely 11.512925465 =
NAME STO RCL PLOT FIND EXIT
```

Full Precision messages show the full precision of the selected parameter value, when   is active.

5. Import Messages

```
R      = 1.0000 kΩ
C      = 1.0000 nF
ts     = 11.5129 μs
Accu   = 11.5129 τ
Accu   = 10.0000 PPM
Accu   = 100.0000 μV
Vstep  = 10.0000 V
τ      = 1.0000 μs
Import value: 5.56776 =
HELP EXP INF RESET FIND EXIT
```

Import messages show the value to be imported.

SECTION 6 - EXAMPLES

This section demonstrates how to use STC by solving a real world problem.

Entering (◀, ▶) and Finding (F5)

STC enables parameters to be entered or found.

In this example, STC is used to predict the settling time of the output voltage of a precision digital to analog convertor (DAC) under different load conditions. Trade-offs between settling time, accuracy, and load are examined. The MAX542A precision DAC is used as an example. The application circuit is shown below,

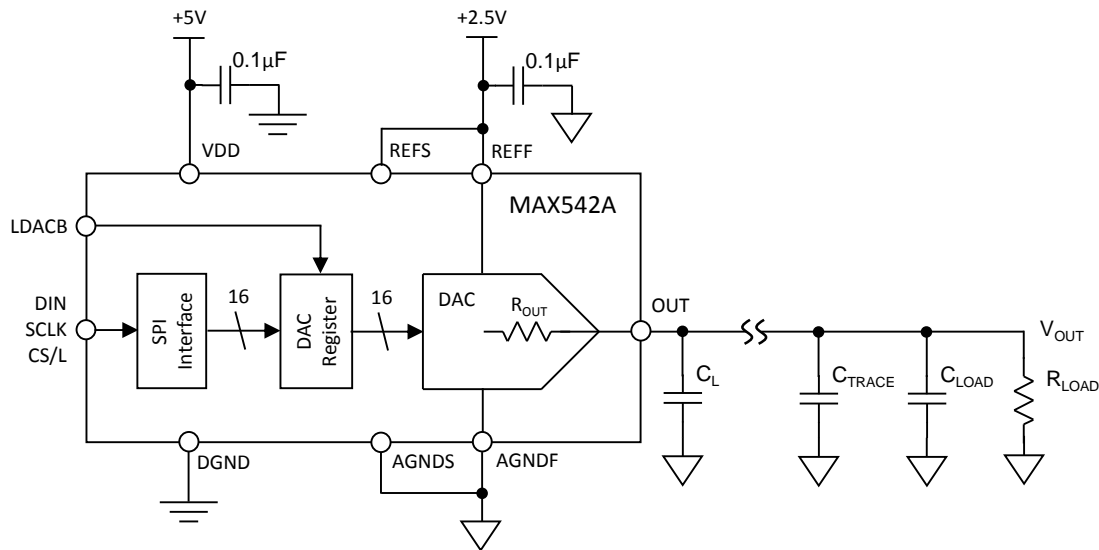


Figure 1

In this circuit, the output voltage (V_{OUT}) settles to a final value defined by the equation,

$$V_{OUT} = V_{REF} \cdot \frac{DIN[15:0]}{2^N}$$

Where,

V_{REF} is the full scale reference voltage, 2.5V

N is the DAC resolution, 16 bits

DIN[15:0] is a user supplied digital code ranging from 0 to 65,535.

R_{OUT} is the DACs output impedance, 6.25kΩ

C_L is the load capacitance specified as the test condition in the data sheet, 10pF

C_{TRACE} is the capacitance due to circuit board trace, vias, connectors, etc.

C_{LOAD} is the load capacitance (i.e., opamp input capacitance)

R_{LOAD} is the load resistance to ground

The falling edge of LDACB ("Load DAC Bar") initiates an output voltage change and is the time zero reference point (t_0) when measuring the settling time (t_s). See Figure 2 below.

Graphically,

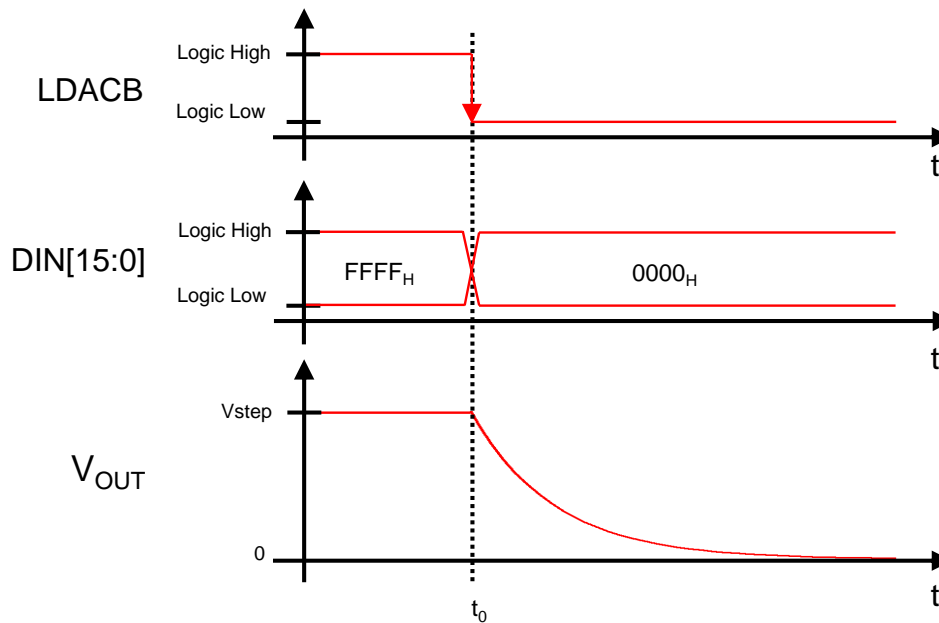


Figure 2

1. Finding the Settling Time Under Device Test Conditions

First, calculate the settling time of MAX542A DAC under the test conditions given in the data sheet.

```

R    = 1.0000 kΩ
C    = 1.0000 nF
ts   = 11.5129 μs
Accu = 11.5129 τ
Accu = 10.0000 PPM
Accu = 100.0000 μV
Vstep = 10.0000 V
τ     = 1.0000 μs
=
HELP EXP INF RESET FIND EXIT

```

Step 1:

Start with STC's default parameter values as shown.

The MAX542A datasheet gives the following device parameters used in this example,

ELECTRICAL CHARACTERISTICS

(VDD = +5V ±5%, VREF = +2.5V, AGND = DGND = 0, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION ($R_L = \infty$)						
Resolution	N		16			Bits
DAC Output Resistance	ROUT	(Note 2)		6.25		kΩ
DYNAMIC PERFORMANCE—ANALOG SECTION ($R_L = \infty$, unipolar mode)						
Output Settling Time		to $\pm 1/2$ LSB of FS, $C_L = 10$ pF		1		μs

Note 2: ROUT tolerance is typically ±20%.

This test condition assumes, in Figure 1, that C_{TRACE} and C_{LOAD} are zero, and R_{LOAD} is infinite.

```

R    = 6.2500 kΩ
C    = 1.0000 nF
ts   = 11.5129 μs
Accu = 11.5129 τ
Accu = 10.0000 PPM
Accu = 100.0000 μV
Vstep= 10.0000 V
τ    = 6.2500 μs
#
NAME STO RCL PLOT FIND EXIT

```

Step 2:

With the selection arrow (↩) pointing to **R**, use the (←) or (→) key to enter the DAC's output resistance, R_{OUT} , into **R**. From the Electrical characteristics table R_{OUT} is 6.25kΩ. Note that the consistency indicator changes from = to ≠ indicating that all parameters are no longer consistent.

```

R    = 6.2500 kΩ
C    = 0.0100 nF
ts   = 11.5129 μs
Accu = 11.5129 τ
Accu = 10.0000 PPM
Accu = 100.0000 μV
Vstep= 10.0000 V
τ    = 0.0625 μs
#
NAME STO RCL PLOT FIND EXIT

```

Step 3:

Use the up and down arrow keys (▼ and ▲) to move the selection arrow (↩) to **C**. Enter the load capacitance, C_L , from the data sheet of 10pF (0.01nF)

```

R    = 6.2500 kΩ
C    = 0.0100 nF
ts   = 11.5129 μs
Accu = 11.5129 τ
Accu = 10.0000 PPM
Accu = 0.0102 LSB
Res  = 10.0000 bit
τ    = 0.0625 μs
#
NAME STO RCL PLOT FIND EXIT

```

Step 4:

Enter the DAC resolution of 16 bits and the specified settling time accuracy of 0.5 LSB. Move the selection arrow (↩) to any of the accuracy (**Accu**) parameters and press the right arrow key (→) to display **Accu** in LSBs and resolution (**Res**) in bits.

```

R    = 6.2500 kΩ
C    = 0.0100 nF
ts   = 11.5129 μs
Accu = 11.7835 τ
Accu = 7.6294 PPM
Accu = 0.5000 LSB
Res  = 16.0000 bit
τ    = 0.0625 μs
#
NAME STO RCL PLOT FIND EXIT

```

Step 5:

First, select **Res** and enter the DAC resolution of 16 bit. Next, select the **Accu** parameter in LSB and enter 0.5. Note that the equivalent accuracies in τ and PPM are automatically updated.

```

R    = 6.2500 kΩ
C    = 0.0100 nF
ts   = 0.7365 μs
Accu = 11.7835 τ
Accu = 7.6294 PPM
Accu = 0.5000 LSB
Res  = 16.0000 bit
τ    = 0.0625 μs
=
NAME STO RCL PLOT FIND EXIT

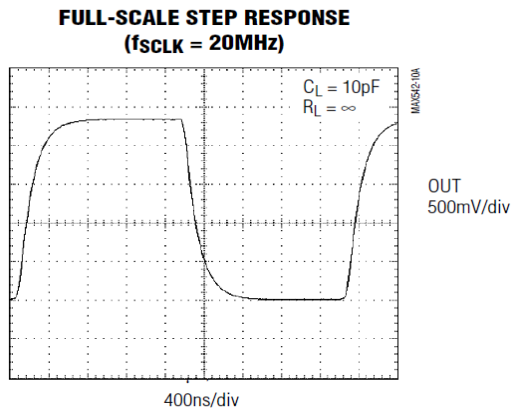
```

Step 6:

Find the settling time by selecting parameter **ts** and pressing the (F5) (□) key. Parameter **ts** changes showing a settling time of 0.74μs. Note that the consistency indicator changed from ≠ to = indicating that all parameters are consistent.

We find that V_{OUT} settles to 0.5 LSB of its final value in 0.74μs. Observe that this is less than the 1μs typical settling time specified in the data sheet. This difference is because the 1μs specification is a conservative estimate accounting for typical process variations (e.g., $R_{OUT} \pm 20\%$)

The predicted settling time of $0.74\mu\text{s}$ is in close agreement with the step response found in the Typical Operating Conditions (TOC) section of the data sheet,



Next, for the same circuit, find the accuracy in μV , given a full scale step of 2.5V.

```

R   = 6.2500 kΩ
C   = 0.0100 nF
ts  = 0.7365 μs
Accu = 11.7835 μV
Accu = 7.6294 PPM
Accu = 76.2939 μV
Vstep = 10.0000 V
τ    = 0.0625 μs
NAME STO RCL PLOT FIND EXIT

```

Step 7:

Display **Accu** in μV and **Vstep** in volts. Move the up and down arrow keys (∇ and Δ) to move the selection arrow (\blacktriangleleft) to any of the accuracy (**Accu**) parameters and press the right arrow key (\blacktriangleright).

```

R   = 6.2500 kΩ
C   = 0.0100 nF
ts  = 0.7365 μs
Accu = 11.7835 μV
Accu = 7.6294 PPM
Accu = 19.0735 μV
Vstep = 2.5000 V
τ    = 0.0625 μs
NAME STO RCL PLOT FIND EXIT

```

Step 8:

Enter the full scale step voltage of 2.5V in **Vstep**. Note that **Accu** in μV automatically changed to $19.07\mu\text{V}$.

We find that V_{OUT} settles to within $19\mu\text{V}$ of its final value in $0.74\mu\text{s}$.

2. Finding the Settling Time Under Real World Conditions

In real application circuits (see Figure 1), the DAC output will see additional capacitance due to the (C_{TRACE}) and load (C_{LOAD}), and additional load resistance (R_{LOAD}). The presence of these will affect the settling time. R_{LOAD} appears in parallel to R_{OUT} effectively reducing R_{OUT} , and C_{TRACE} and C_{LOAD} add to C_L increasing the effective load capacitance (Figure 3).

In this second example, find the settling time of the MAX542A DAC when driving a high impedance input of an OpAmp ($R_{\text{LOAD}} = \infty$) having 5pF input capacitance ($C_{\text{LOAD}} = 5\text{pF}$) and a trace capacitance of 20 pF ($C_{\text{TRACE}} = 20\text{pF}$).

```

R   = 6.2500 kΩ
C   = 0.0350 nF
ts  = 0.7365 μs
Accu = 11.7835 τ
Accu = 7.6294 PPM
Accu = 19.0735 μV
Vstep = 2.5000 V
τ   = 0.2188 μs
#
NAME STO RCL PLOT FIND EXIT

```

Step 9:

Use the up and down arrow keys (∇ and \triangle) to move the selection arrow (\blacklozenge) to **C**. Enter the total load capacitance of 35pF (0.035nF), $C = C_L + C_{TRACE} + C_{LOAD} = 10\text{pF} + 20\text{pF} + 5\text{pF}$.

```

R   = 6.2500 kΩ
C   = 0.0350 nF
ts  = 2.5776 μs
Accu = 11.7835 τ
Accu = 7.6294 PPM
Accu = 19.0735 μV
Vstep = 2.5000 V
τ   = 0.2188 μs
=
NAME STO RCL PLOT FIND EXIT

```

Step 10:

Find the settling time by moving the selection arrow (\blacklozenge) to **ts**. and pressing the $F5$ (||||) key. The settling time has more than tripled to 2.6μs.

It is seen that, although the MAX542A data sheet specifies a typical settling time of 1μs, it can be much longer under the load conditions found in a typical application circuit.

3. Finding the Output Accuracy Under Load

Find the accuracy, in uV and LSB, to which the application circuit will settle in 1μs.

```

R   = 6.2500 kΩ
C   = 0.0350 nF
ts  = 1.0000 μs
Accu = 11.7835 τ
Accu = 7.6294 PPM
Accu = 19.0735 μV
Vstep = 2.5000 V
τ   = 0.2188 μs
#
NAME STO RCL PLOT FIND EXIT

```

Step 11:

Enter 1μs in **ts**.

```

R   = 6.2500 kΩ
C   = 0.0350 nF
ts  = 1.0000 μs
Accu = 4.5714 τ
Accu = 10343.173 PPM
Accu = 25857.933 μV
Vstep = 2.5000 V
τ   = 0.2188 μs
=
NAME STO RCL PLOT FIND EXIT

```

Step 12:

Find **Accu** in PPM.

```

R   = 6.2500 kΩ
C   = 0.0350 nF
ts  = 1.0000 μs
Accu = 4.5714 τ
Accu = 1.0343 %
Accu = 677.8502 LSB
Res  = 16.0000 bit
τ   = 0.2188 μs
=
NAME STO RCL PLOT FIND EXIT

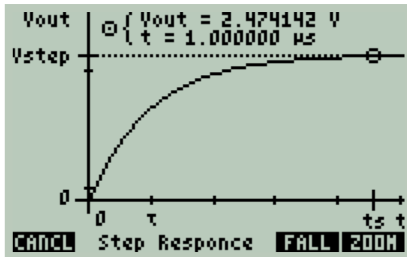
```

Step 13:

Display **Accu** in % and LSB by pressing the right arrow key (\blacktriangleright) at PPM (to display %) and again at **Accu** in μV to display **Accu** in LSB.

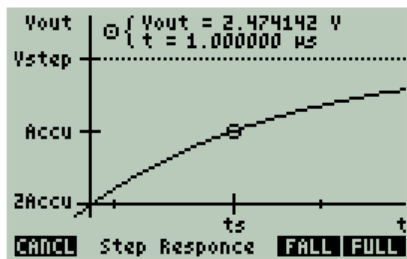
Settling time can be very sensitive to load capacitance. Here, it is found that tripling the load capacitance (10pF to 35pF) reduces the accuracy at 1 μ s by over a factor of 1000 (0.5LSB to 677 LSB)!

Plotting (F4)




Step 14:

Press **F4** to plot the step response. The parameters must be consistent (i.e., “=” displayed) to be plotted.

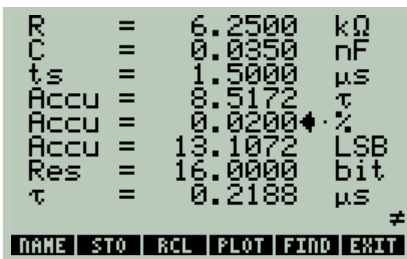


Step 15:

Press **F6** () to zoom in around **ts**.

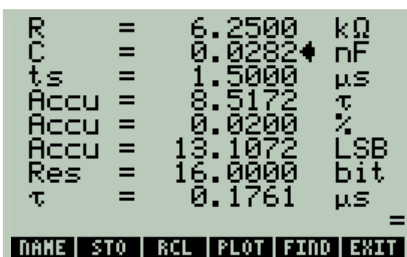
4. Finding the Maximum Load Capacitance

Finally, find the maximum load capacitance that can be driven and achieve an accuracy of 0.02% in 1.5 μ s.



Step 16:

Enter 1.5μs in **ts** and 0.02% in **Accu**,



Step 17:

Find **C**.

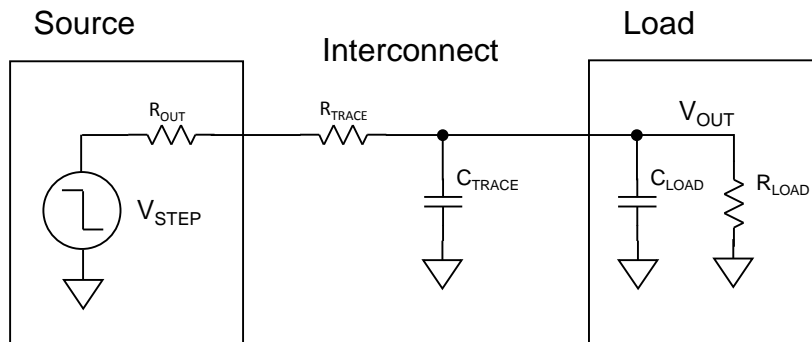
It is found that to settle within $1.5\mu s$ the total load capacitance must be less than or equal to $28pF$.

SECTION 7 - BACKGROUND

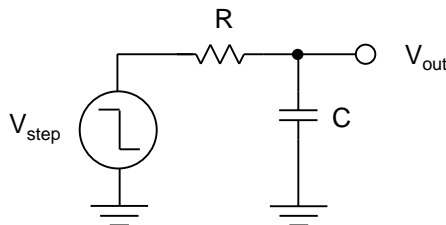
All electrical circuits suffer from some degree of time delay between input excitation and output response. This delay limits both the speed of digital circuits and the precision of analog circuits. This delay is often measured as the time it takes for the output voltage to respond to a step change in input voltage.

The RC Network

Common causes of signal delay are the RC networks found in every circuit. They are made from the various resistances and capacitances found in all signal sources, interconnections, and loads. For example,



These resistances and capacitances can be combined, and the circuit reduced to a simplified RC network as shown,



Where,

$$R = \frac{R_{OUT} \cdot (R_{TRACE} + R_{LOAD})}{R_{OUT} + R_{TRACE} + R_{LOAD}}$$

$$\text{and, } C = C_{TRACE} + C_{LOAD}$$

Figure 3

The step response of this circuit is an exponentially declining output voltage, given by the equation,

$$V_{OUT} = V_{STEP} \cdot e^{-\frac{t}{\tau}}$$

Where τ is the time constant, $\tau = R \cdot C$. The settling time increases with R and C.

Accuracy vs. Settling Time

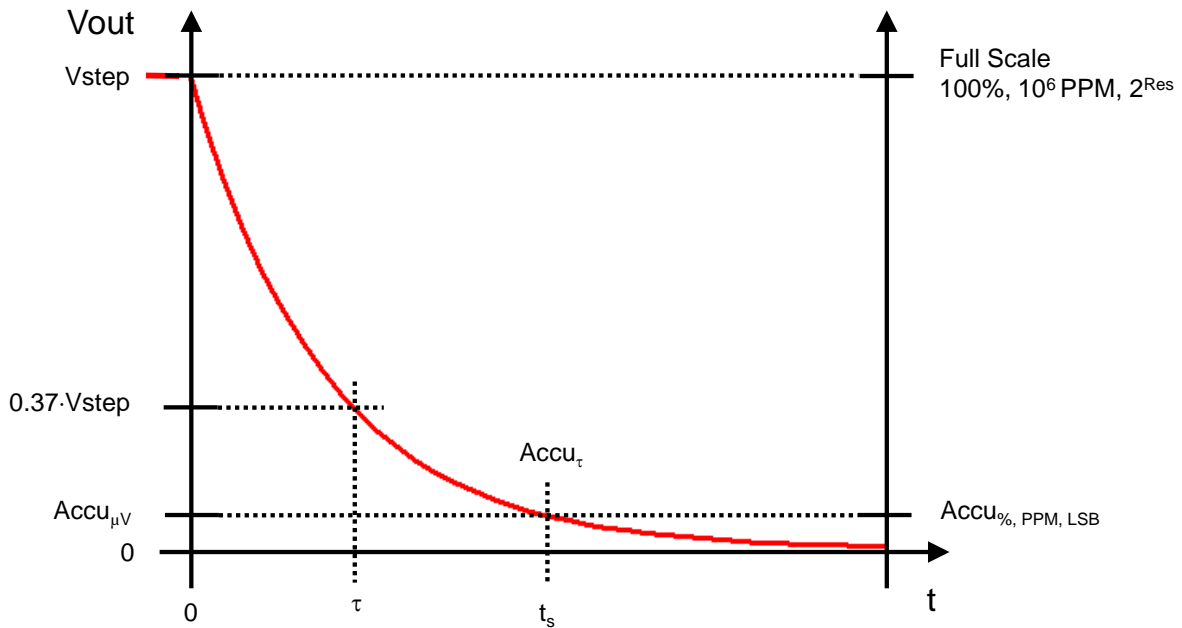
How close V_{OUT} comes to its final value (0V) is a measure of accuracy, and is specified at a particular time, t_s . Accuracy is usually measured as a fraction of the step size, V_{STEP} .

$$\frac{V_{OUT}}{V_{STEP}} = e^{-\frac{t_s}{RC}} = \frac{Accu_{\mu V}}{V_{STEP}}$$

Accuracy may be expressed in several of ways. STC uses five: μV , LSB, %, PPM, or number of τ s. These parameters are related by the equation,

$$e^{-\frac{t_s}{RC}} = e^{-Accu_{\tau}} = \frac{Accu_{\mu V}}{V_{STEP}} = \frac{Accu_{\%}}{100} = \frac{Accu_{PPM}}{1000000} = \frac{Accu_{LSB}}{2^{Res}}$$

Graphically,



As can be seen, the greater the accuracy the longer it takes to settle.

The settling time of an RC network is commonly defined to be 5τ , where V_{OUT} settles to less than 1% of its final value. However, settling time can be two or three times longer than this for high accuracy circuits such as 12 to 20 bit precision DACs. This can be seen in the following table that shows equivalent measures of accuracy.

Table of Equivalent Accuracy

Equivalent Accuracy				
τ	%	PPM	μV^*	bits **
0.0	100.0000000	1000000.000	4096000.0000	0.0
0.7	50.0000000	500000.000	2048000.0000	1.0
1.0	36.7879441	367879.441	1506834.1910	1.4
2.0	13.5335283	135335.283	554333.3201	2.9
3.0	4.9787068	49787.068	203927.8320	4.3
4.0	1.8315639	18315.639	75020.8569	5.8
4.6	1.0000000	10000.000	40960.0000	6.6
5.0	0.6737947	6737.947	27598.6309	7.2
5.5	0.3906250	3906.250	16000.0000	8.0
6.0	0.2478752	2478.752	10152.9689	8.7
6.9	0.0976563	976.563	4000.0000	10.0
7.0	0.0911882	911.882	3735.0685	10.1
8.0	0.0335463	335.463	1374.0549	11.5
8.3	0.0244141	244.141	1000.0000	12.0
9.0	0.0123410	123.410	505.4866	13.0
9.7	0.0061035	61.035	250.0000	14.0
10.0	0.0045400	45.400	185.9581	14.4
11.0	0.0016702	16.702	68.4102	15.9
11.1	0.0015259	15.259	62.5000	16.0
12.0	0.0006144	6.144	25.1667	17.3
12.5	0.0003815	3.815	15.6250	18.0
13.0	0.0002260	2.260	9.2583	18.8
13.9	0.0000954	0.954	3.9063	20.0
14.0	0.0000832	0.832	3.4059	20.2
15.0	0.0000306	0.306	1.2530	21.6
15.2	0.0000238	0.238	0.9766	22.0
16.0	0.0000113	0.113	0.4609	23.1
16.6	0.0000060	0.060	0.2441	24.0
17.0	0.0000041	0.041	0.1696	24.5

* $V_{STEP} = 4.096V$

** 1 LSB accuracy

Rise Time

Rise time, t_r , is commonly defined as the time it takes V_{OUT} to move from 10% to 90% of V_{STEP} . It is calculated by,

$$t_r = \ln(9)RC$$

Bandwidth

The RC network forms a single-pole low-pass filter with a 3dB cut-off frequency, F_c . Where,

$$F_c = \frac{1}{2\pi RC}$$

SECTION 8 - TOOLS, MODELS, AND SOFTWARE NOTICE

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